WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a MOS transistor formed on a semiconductor substrate;

an interlayer insulating film formed on the semiconductor substrate such that the interlayer insulating film covers the MOS transistor;

a contact plug formed in the interlayer insulating film and connected to an impurity diffusion layer of the MOS transistor;

a capacitor lower electrode formed on the contact plug;

a ferroelectric film formed on the capacitor lower electrode; and

two capacitor upper electrodes formed on the capacitor lower electrode with the ferroelectric film interposed therebetween, a contact area between the contact plug and the capacitor lower electrode being greater than a contact area between each of the two capacitor upper electrodes and the ferroelectric film, and at least a part of a gate electrode of the MOS transistor being located just below a region of the contact plug, which region is in contact with the capacitor lower electrode.

2. The semiconductor device according to claim 1, wherein the capacitor lower electrode includes first and second electrode portions which are formed on the

contact plug and separated from each other, and

the two capacitor upper electrodes are formed on the first and second electrode portions, with the ferroelectric film interposed therebetween.

3. The semiconductor device according to claim 1, wherein the contact area between the contact plug and the capacitor lower electrode is at least 1.1 times the contact area between the capacitor upper electrode and the ferroelectric film.

4. The semiconductor device according to claim 1, wherein the contact area between the contact plug and the capacitor lower electrode is double or more greater than the contact area between each of the two capacitor upper electrodes and the ferroelectric film.

5. The semiconductor device according to claim 1, wherein the contact area between the contact plug and the capacitor lower electrode is less than an area of a surface of the capacitor lower electrode, which surface faces the contact plug.

6. The semiconductor device according to claim 1, wherein the capacitor lower electrode includes a metal element belonging to the platinum group.

7. The semiconductor device according to claim 1, further comprising:

a silicide film formed between the capacitor lower electrode and the contact plug.

8. The semiconductor device according to claim 1,

further comprising:

a first interconnecting metal layer formed by RIE and connected to the capacitor upper electrode; and

a second interconnecting metal layer formed by a damascene process and located above the first metal interconnecting layer.

9. The semiconductor device according to claim 1, wherein the MOS transistor and a capacitor element including the capacitor lower electrode, the ferroelectric film and the capacitor upper electrode constitute a unit cell of the series connected TC unit type ferroelectric RAM.

10. The semiconductor device according to claim 1, wherein a side surface of the capacitor lower electrode, a side surface of the ferroelectric film, and a side surface of the capacitor upper electrode exist on the same plane.

11. The semiconductor device according to claim 1, wherein the contact plug is formed of at least one kind selected from the group including polysilicon, tungsten, Ti_xN_y, $Ti_xAl_yN_z$, W_xN_y, iridium, IrO_x, platinum, Pt_xO_y, $SrRuO_3$, Co_xSi_y, Ti_xSi_y, $Ti_xAl_yO_z$, and $TiAl_xN_yO_z$.

12. A semiconductor device comprising:

two MOS transistors formed on a semiconductor substrate and sharing one of source and drain regions thereof;

an interlayer insulating film formed on the semiconductor substrate such that the interlayer insulating film covers the MOS transistors;

a contact plug including a first plug portion formed in the interlayer insulating film and connected to one of the source and drain regions shared by the two MOS transistor, and a second plug portion formed on the first plug portion and extending from a region of contact with the first plug portion to a region above at least a part of a gate electrode of each of the two MOS transistors;

a capacitor lower electrode formed on the second plug portion of the contact plug;

a ferroelectric film formed on the capacitor lower electrode; and

two capacitor upper electrodes formed on the ferroelectric film, each of the two capacitor upper electrodes overlapping at least a part of the gate electrode of an associated one of the MOS transistors, a contact area between the second plug portion and the capacitor lower electrode being greater than a contact area between each of the two capacitor upper electrodes and the ferroelectric film.

13. The semiconductor device according to claim 12, wherein the contact area between the contact plug and the capacitor lower electrode is less than an area of a surface of the capacitor lower electrode,

which surface faces the contact plug.

14. The semiconductor device according to claim 12, wherein the capacitor lower electrode includes a metal element belonging to the platinum group.

15. The semiconductor device according to claim 12, further comprising:

a silicide film formed between the capacitor lower electrode and the contact plug.

16. The semiconductor device according to claim 12, wherein the MOS transistor and a capacitor element including the capacitor lower electrode, the ferroelectric film and the capacitor upper electrode constitute a unit cell of the series connected TC unit type ferroelectric RAM.

17. The semiconductor device according to claim 12, further comprising:

a first interconnecting metal layer formed by RIE and connected to the capacitor upper electrode; and

a second interconnecting metal layer formed by a damascene process and located above the first metal interconnecting layer.

18. The semiconductor device according to claim 12, wherein a side surface of the capacitor lower electrode, a side surface of the ferroelectric film, and a side surface of the capacitor upper electrode exist on the same plane.

19. The semiconductor device according to claim 12, wherein the contact plug is formed of at least one kind selected from the group including of polysilicon, tungsten, Ti_xN_y, $Ti_xAl_yN_z$, W_xN_y, iridium, IrO_x, platinum, Pt_xO_y, $SrRuO_3$, Co_xSi_y, Ti_xSi_y, $Ti_xAl_yO_z$, and $TiAl_xN_yO_z$.

20. A method for fabricating a semiconductor device comprising:

forming a MOS transistor on a semiconductor substrate;

forming a first interlayer insulating film on the semiconductor substrate, the first interlayer insulating film covering the MOS transistor;

forming a contact plug in the first interlayer insulating film, the contact plug being connected to an impurity diffusion layer of the MOS transistor;

forming a capacitor lower electrode on the contact plug;

forming a ferroelectric film on the capacitor lower electrode; and

forming two capacitor upper electrodes on the capacitor lower electrode with the ferroelectric film interposed therebetween, a contact area between the contact plug and the capacitor lower electrode being greater than a contact area between each of the two capacitor upper electrodes and the ferroelectric film, and a region of the contact plug, which region is in

contact with the capacitor lower electrode, being located just above at least a part of a gate electrode of the MOS transistor.

21. The method according to claim 20, wherein forming the capacitor lower electrode includes:

forming a conductive layer on the first interlayer insulating film and the contact plug; and

patterning the conductive layer and forming first and second electrode portions on the contact plug, the first and second electrode portions being separated from each other, and

the two capacitor upper electrodes are formed on the first and second electrode portions, with the ferroelectric film interposed therebetween.

22. The method according to claim 20, wherein forming the contact plug includes:

making a trench in a surface portion of the first interlayer insulating film;

making a contact hole in the first interlayer insulating film, the contact hole having an open end located in the trench and having a bottom reaching the impurity diffusion layer;

forming a plug material on the first interlayer insulating film, thus burying the plug material in the contact hole and the trench; and

polishing the plug material using the first interlayer insulating film as a stopper, thereby

leaving the plug material only in the contact hole and the trench.

23. The method according to claim 20, wherein forming the contact plug includes:

making a contact hole in the first interlayer insulating film, the contact hole having a depth not reaching the impurity diffusion layer;

etching a surface of the first interlayer insulating film, thus forming a trench including an open end of the contact hole, and at the same time etching a bottom portion of the contact hole such that the bottom portion of the contact hole reaches the impurity diffusion layer;

forming a plug material on the first interlayer insulating film, thus burying the plug material in the contact hole and the trench; and

polishing the plug material using the first interlayer insulating film as a stopper, thereby leaving the plug material only in the contact hole and the trench.

24. The method according to claim 20, wherein forming the contact plug includes:

forming a contact hole in the first interlayer insulating film, the contact hole reaching the impurity diffusion layer;

burying a first plug material in the contact hole, thus forming a first plug;

forming a second interlayer insulating film on the first interlayer insulating film;

forming a trench in the second interlayer insulating film, the trench having a depth reaching the first interlayer insulating film, and exposing the first plug in the trench; and

burying a second plug material in the trench, thus forming a second plug.

25. The method according to claim 24, wherein the first and second plug materials are different materials.

26. The method according to claim 24, wherein the first and second plug materials are the same material.

27. The method according to claim 22, wherein the trench is formed to overlap at least a part of a gate electrode of the MOS transistor.

28. The method according to claim 23, wherein the trench is formed to overlap at least a part of a gate electrode of the MOS transistor.

29. The method according to claim 24, wherein the trench is formed to overlap at least a part of a gate electrode of the MOS transistor.

30. The method according to claim 20, further comprising:

performing RIE after forming the two capacitor upper electrodes, thereby forming first interconnecting metal layers which are connected to the two capacitor

upper electrodes, respectively; and

performing a damascene process, thereby forming a second interconnecting metal layer at a level higher than the first metal interconnecting layers.